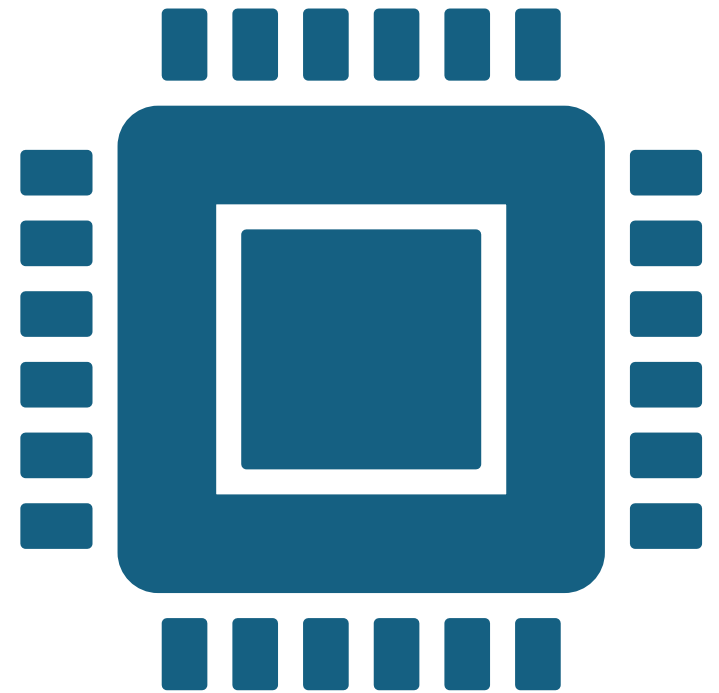


CPU - Smart zariadenia - riadiaca jednotka, inštrukčné sady, registre, komunikácia

Michal Borák

3.Aplikovaná Informatika

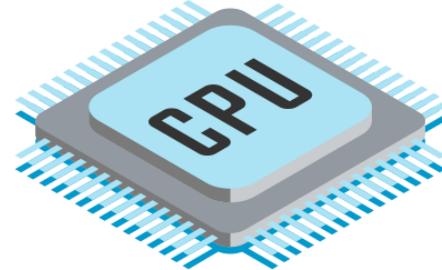


Úvod do témy

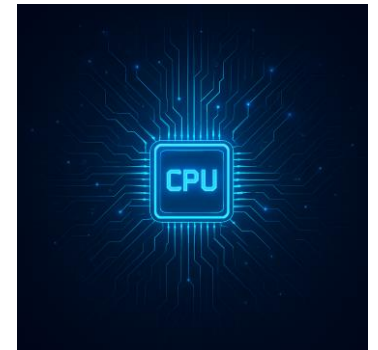
CPU = Základ smart zariadení



Riadi výpočty a komunikáciu

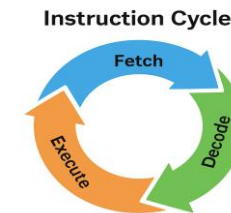


Téma: Fungovanie, história,
súčasnosť, budúcnosť,
diagnostika

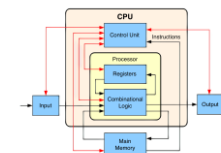


Princíp fungovania CPU

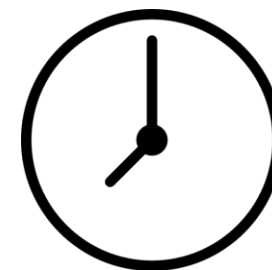
Inštrukčný cyklus: Fetch –Decode–Execute



Časti CPU: ALU, riadiaca jednotka, registre



Hodinový signál (Clock)



Instrukční
sady a
registre

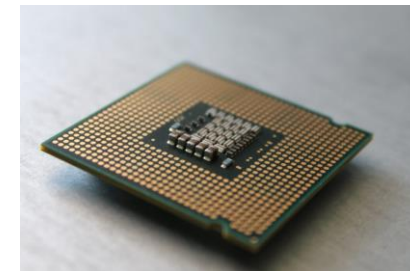
RISC vs CISC

CISC	RISC
• Emphasis on hardware • Multiple instruction sizes and formats • Less registers • More addressing modes • Extensive use of microprogramming • Instructions take a varying amount of cycle time • Pipelining is difficult	• Emphasis on software • Instructions of same set with few formats • Uses more registers • Fewer addressing modes • Complexity in compiler • Instructions take one cycle time • Pipelining is easy

ARM, x86



PC, IR, ACC,
všeobecné registre



Historické mílniky

2007 – iPhone: ARM11 (Samsung S5L8900)



2010 – Apple A4 (prvý vlastný čip Apple)

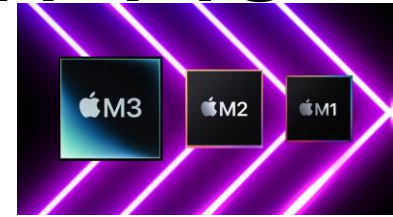
2010 – Qualcomm Snapdragon S1 (Android zariadenia)

2011 – Samsung Exynos 4210 (dvojjadrový mobilný čip)

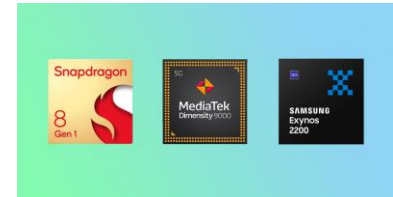
2014 – MediaTek MT6592 (prvý 8-jadrový čip)

Súčasn^é CPU

Apple M1 / M2 / M3



Snapdragon, MediaTek, Exynos



ARM – efektívnosť, viac jadier, AI akcelerácia

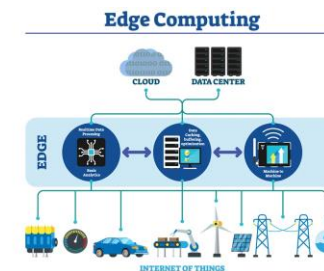


Budúcnosť
CPU

AI a neurónové jadrá



Edge computing



Vyššia efektivita, nižšia
spotreba



Diagnostika a správa

CPU-Z, AIDA64,
HWMonitor

BIOS: taktovanie,
napätie

Testy: Prime95,
Cinebench

Záver

CPU = Riadiaci mozog
Smart zariadení

Vývoj od Intel 4004 po
neurónové čipy

Budúcnosť: inteligentné,
úsporné CPU

Zdroje

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